30 nm $In_{0.7}Ga_{0.3}As$ Inverted-type HEMT with Reduced Gate Leakage Current for Logic Applications

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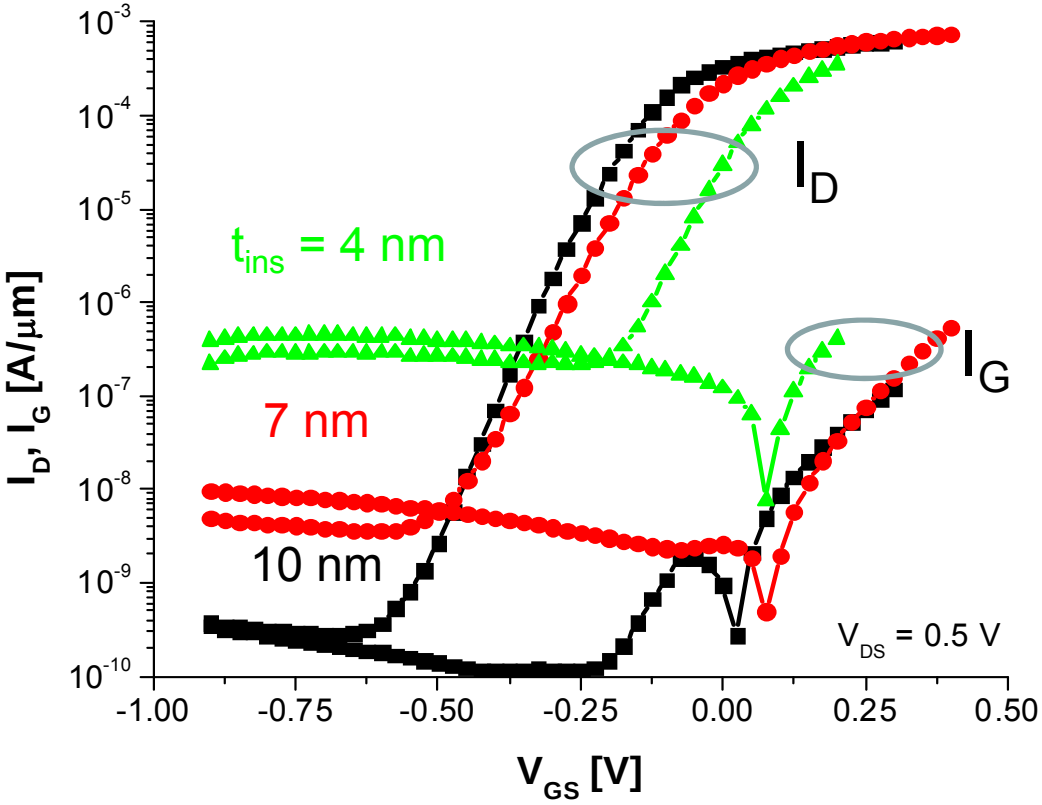
Outline

1. Introduction
2. Device Technology
3. Logic Characteristics
4. Benchmarking with normal HEMT and Si CMOS
5. Conclusions

Insulator Scaling in III-V HEMTs

Motivation : - III-V HEMT: Model system for future III-V logic FETs

- HEMT scaling: $L_g \downarrow \rightarrow t_{ins} \downarrow$
- Problem: $t_{ins} \downarrow \rightarrow I_G \uparrow$



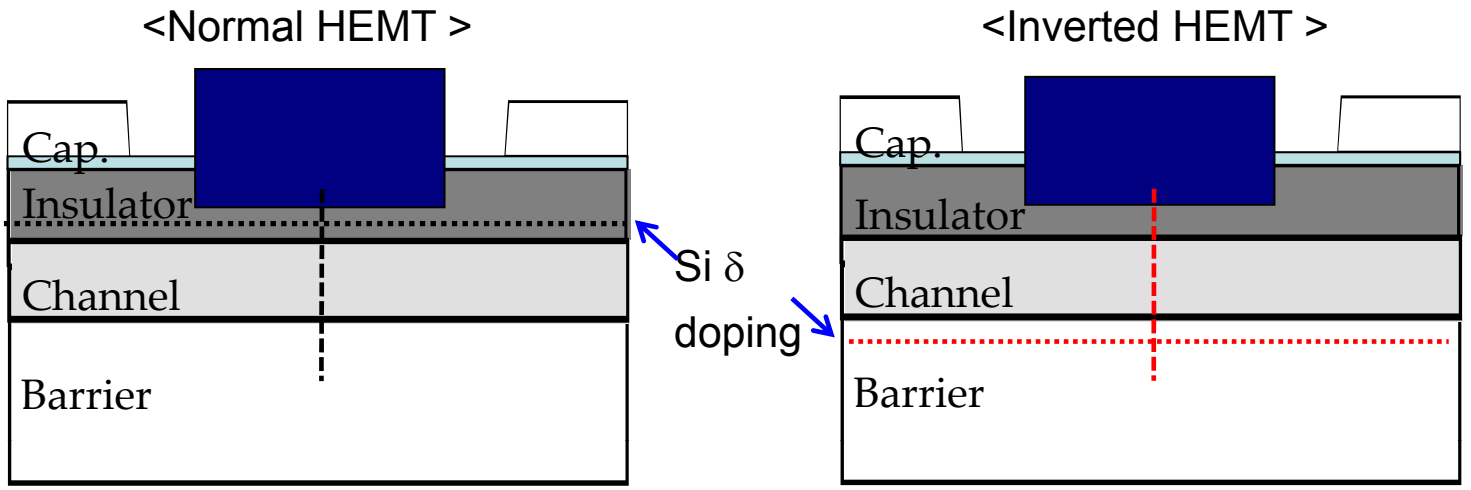
InAlAs/InGaAs HEMT

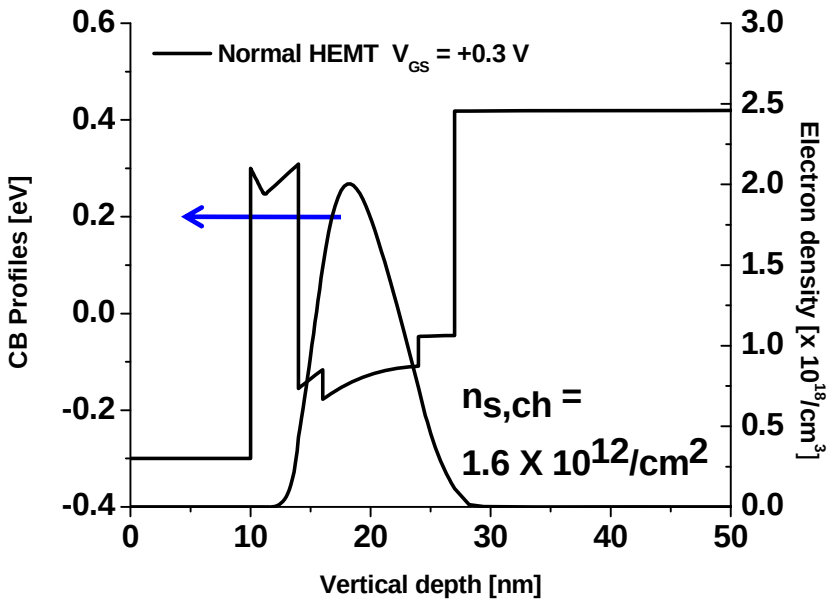
L_g = 30 nm

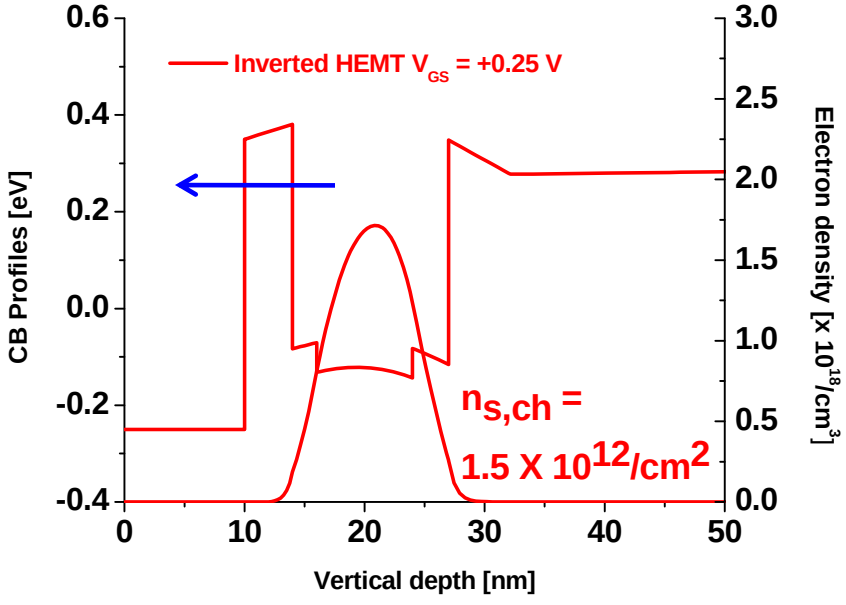
<del Alamo, TWHM 09>

- Inverted HEMT design: reduced I_G

Concept of Inverted HEMT

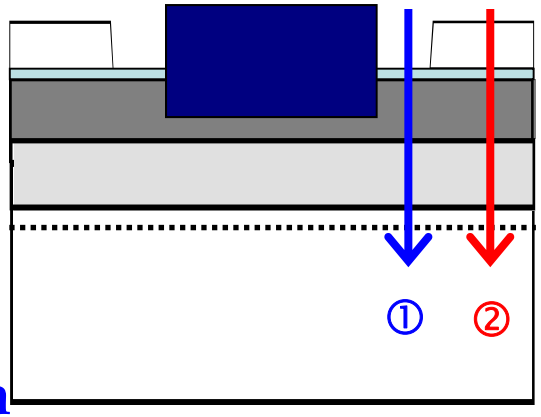




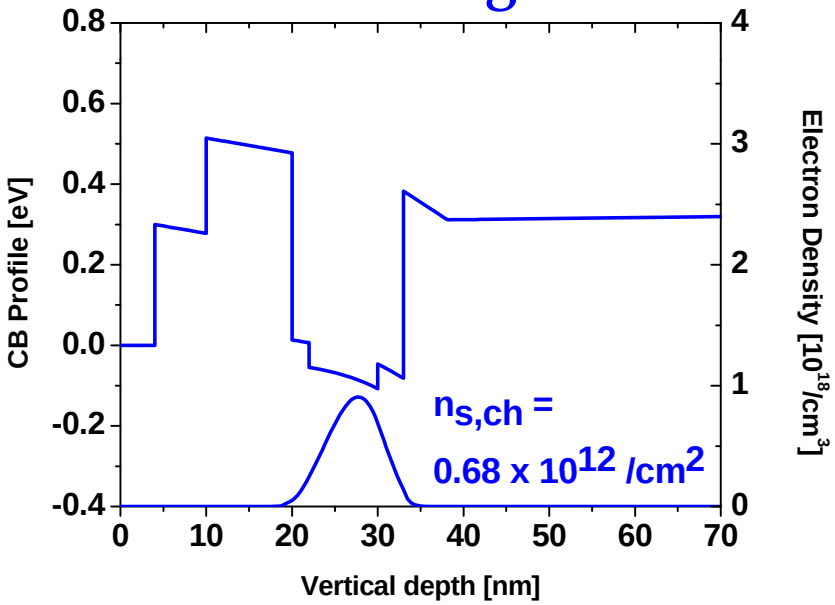


- Lower leakage current due to higher barrier under gate

Trade-off of Inverted HEMT

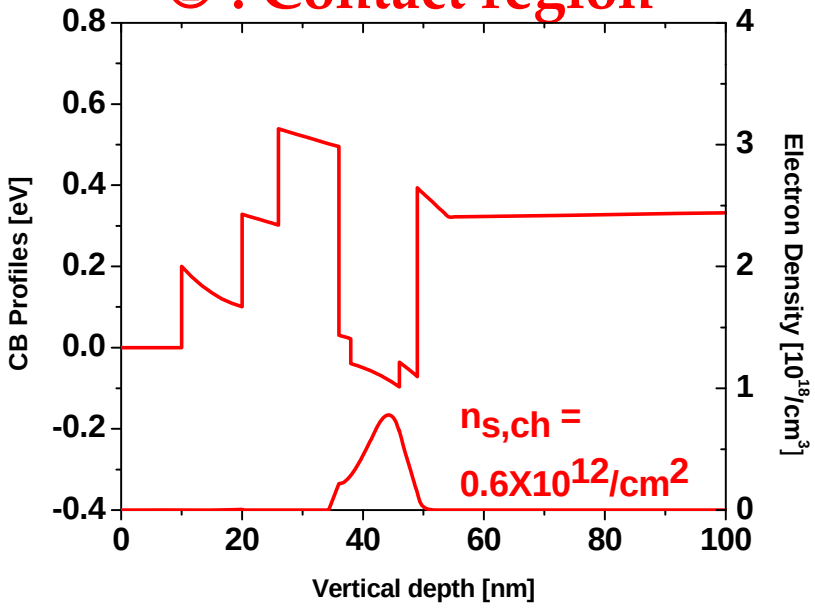


① : Access region



$n_{s.ch}$ ~ 2.7 x 10^{12}/cm^2 for Normal HEMT

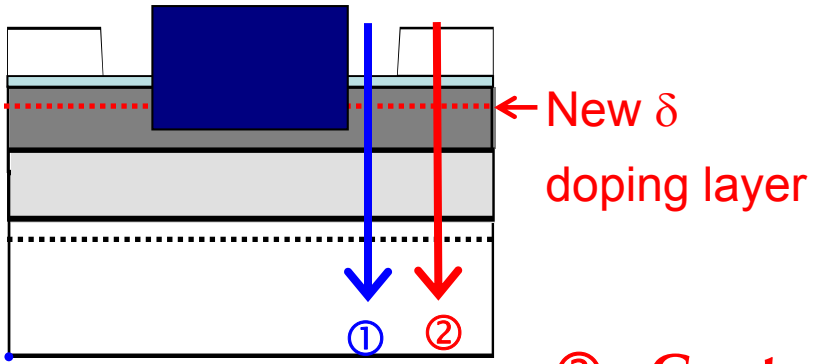
② : Contact region



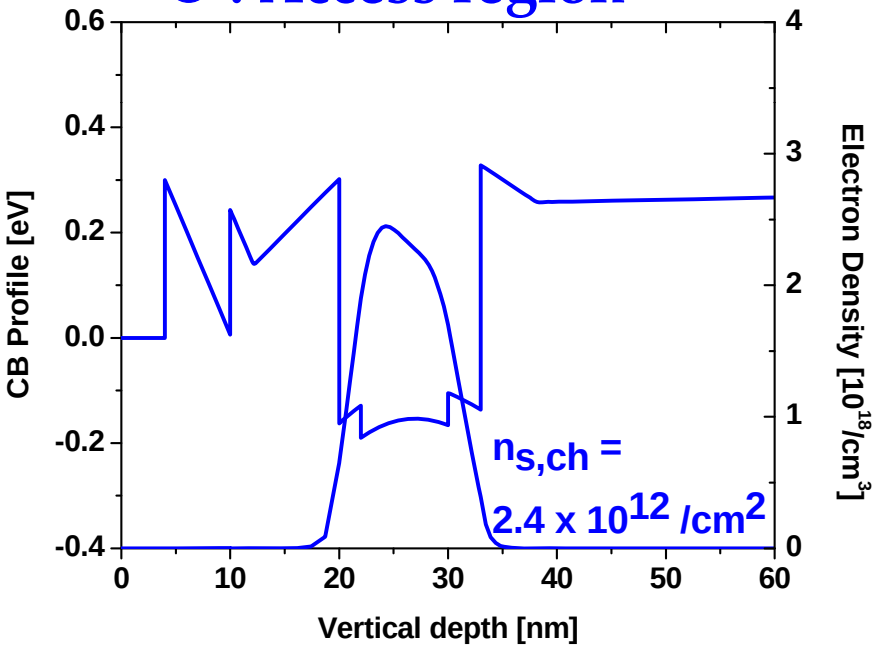
$n_{s,ch}$ ~ 3 x 10^{12}/cm^2 for Normal HEMT

- Problem: - low n_s in access region
  - large energy barrier under contact region

New Approach

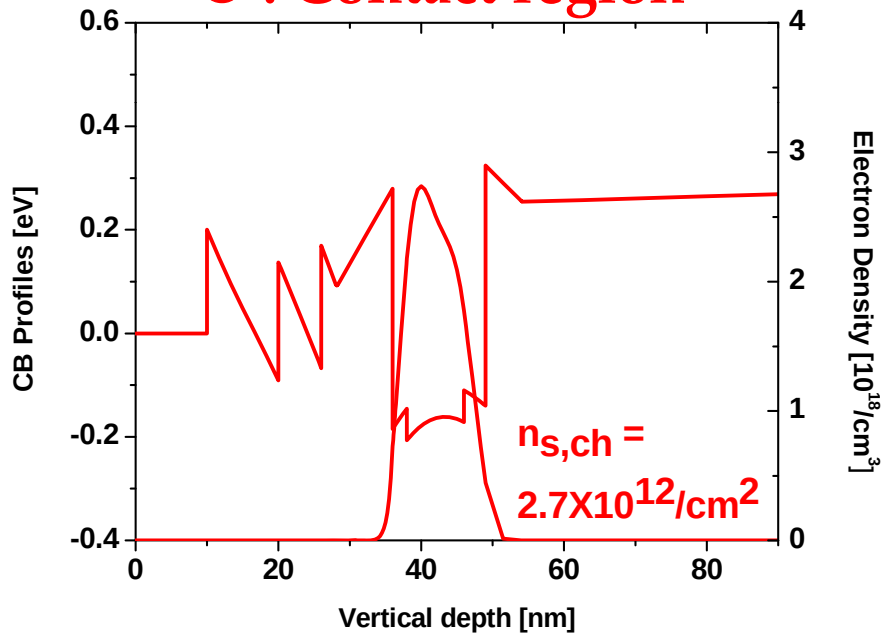


① : Access region



$n_{s.ch}$ ~ 2.7 x 10^{12}/cm^2 for Normal HEMT

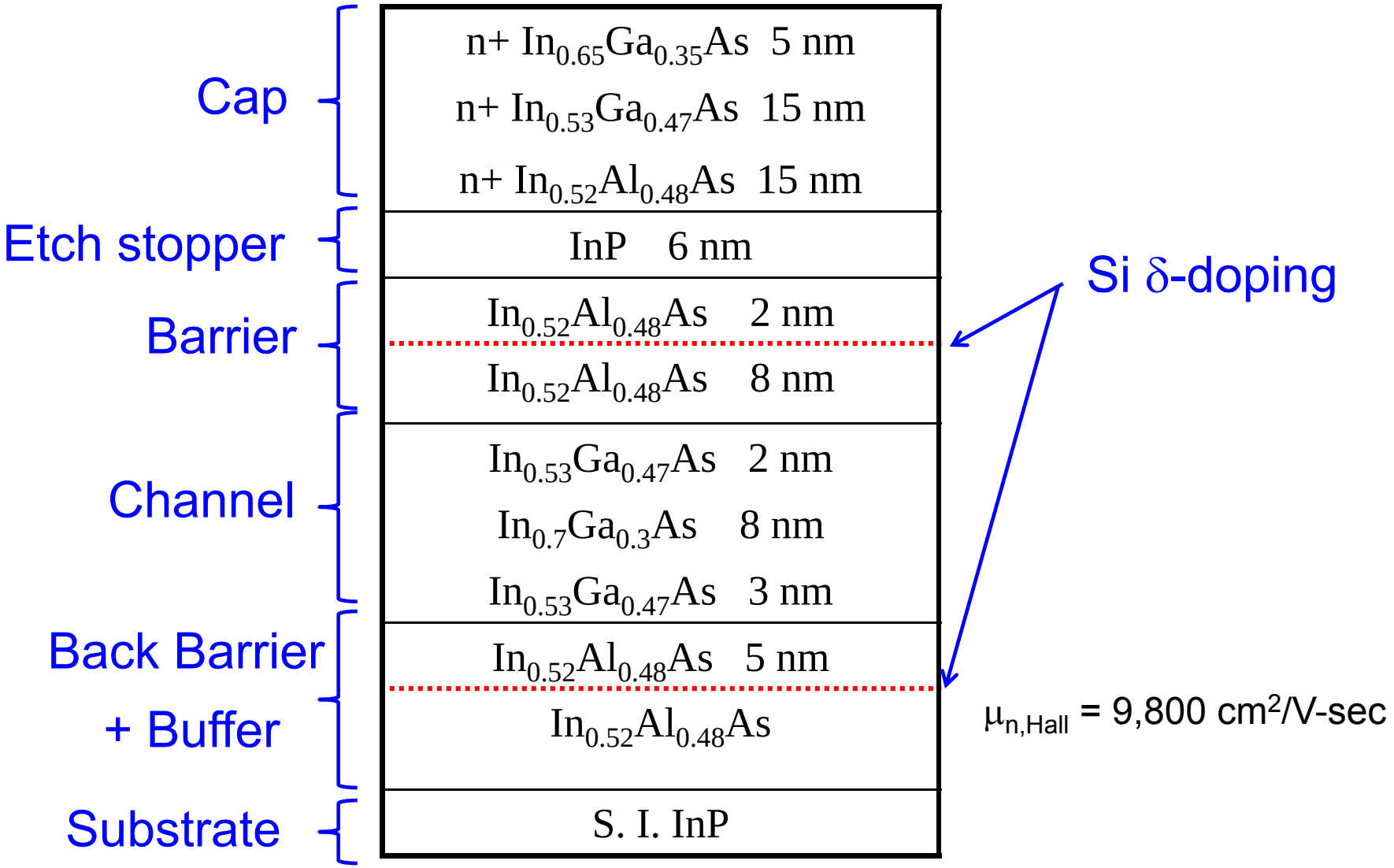
② : Contact region



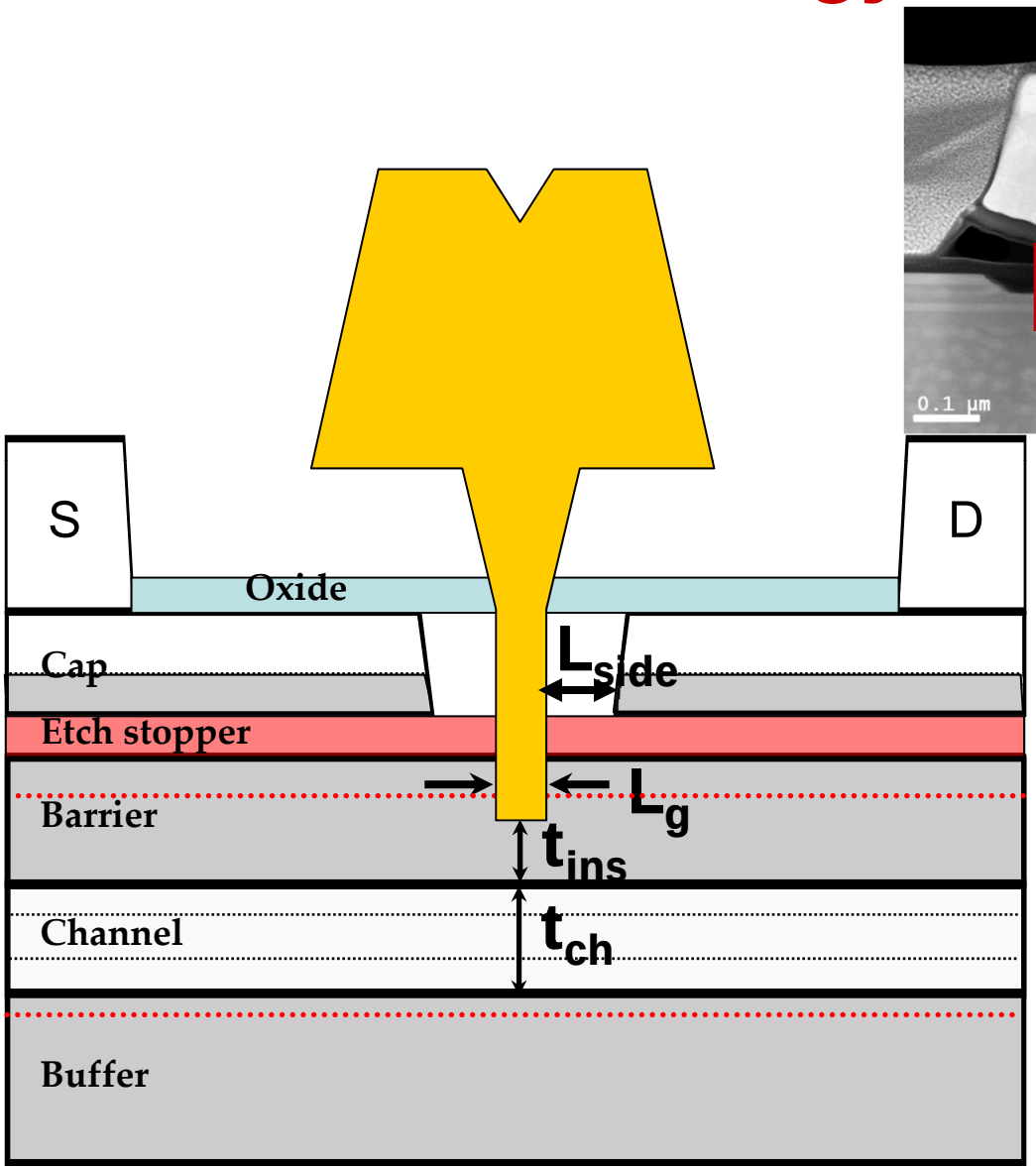
$n_{s,ch}$ ~ 3 x 10^{12}/cm^2 for Normal HEMT

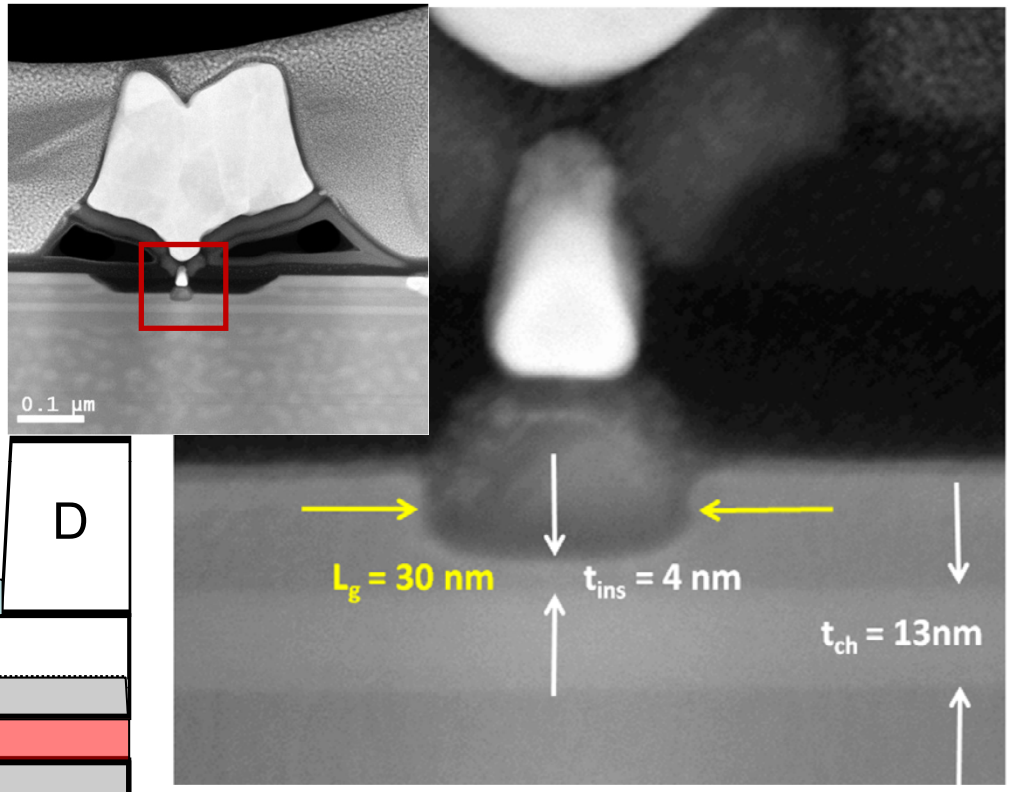
- High n_s in access region
- Low barrier in contact region

Epitaxial Heterostructure



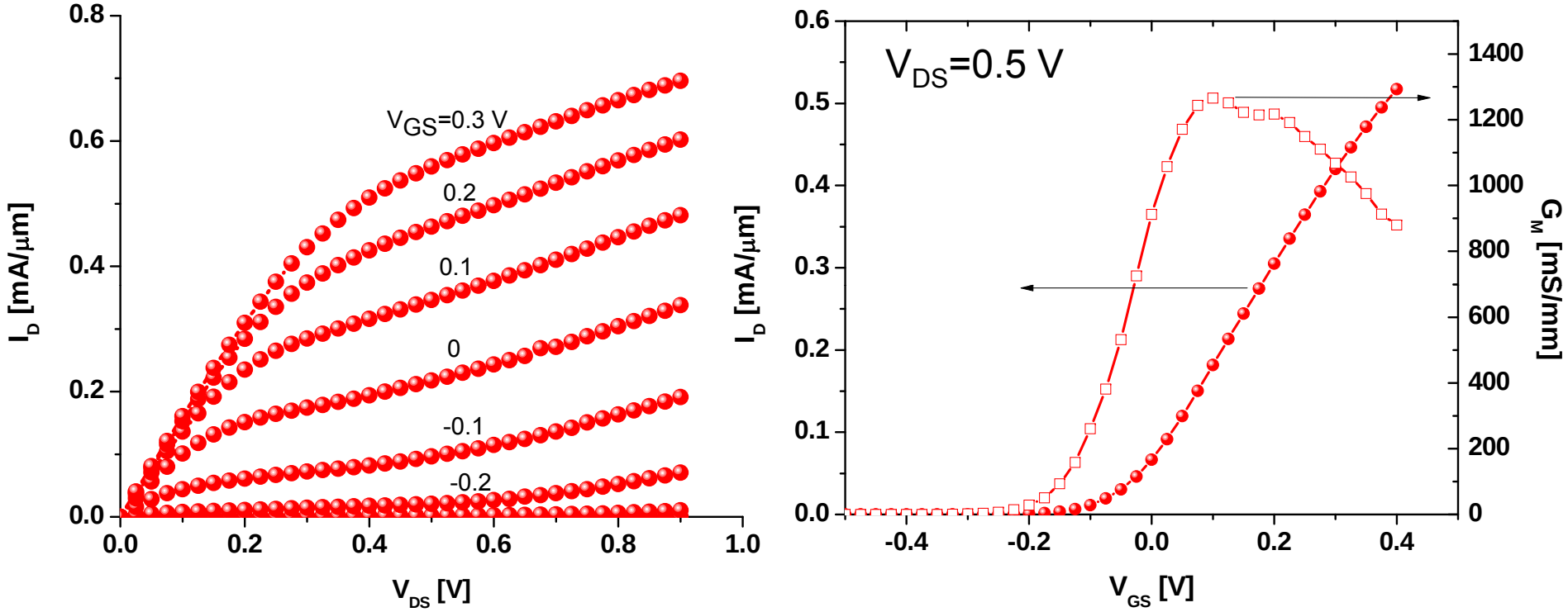
Device Technology





- Triple-recess process
- t_{ins} = 4 nm, L_{side} = 80 nm
- Gate: Ti/Pt/Au
- L_g: 30 - 130 nm

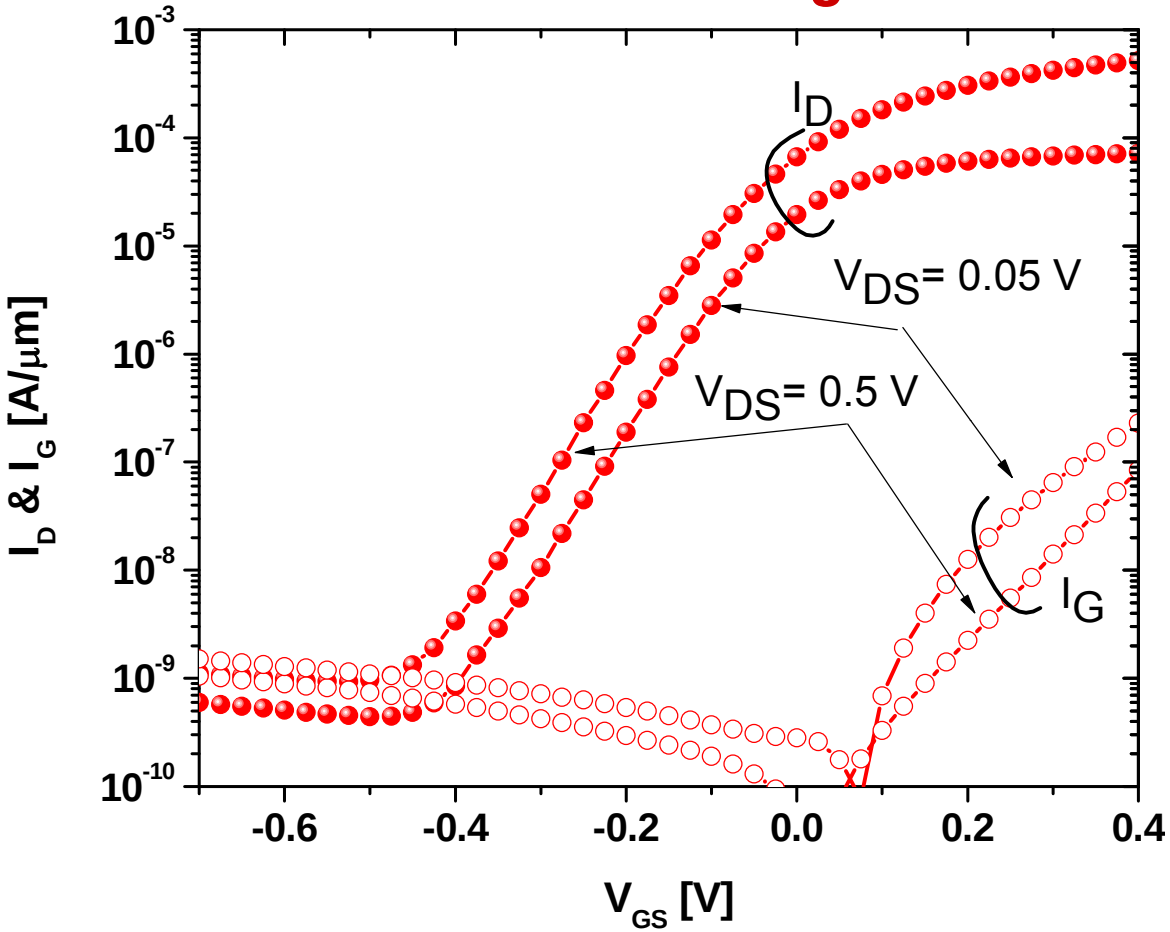
Output & Transfer Char. : L_G = 30 nm



Good I_D saturation, pinch-off behavior

G_m = 1.27 S/mm @ V_{DS}=0.5 V

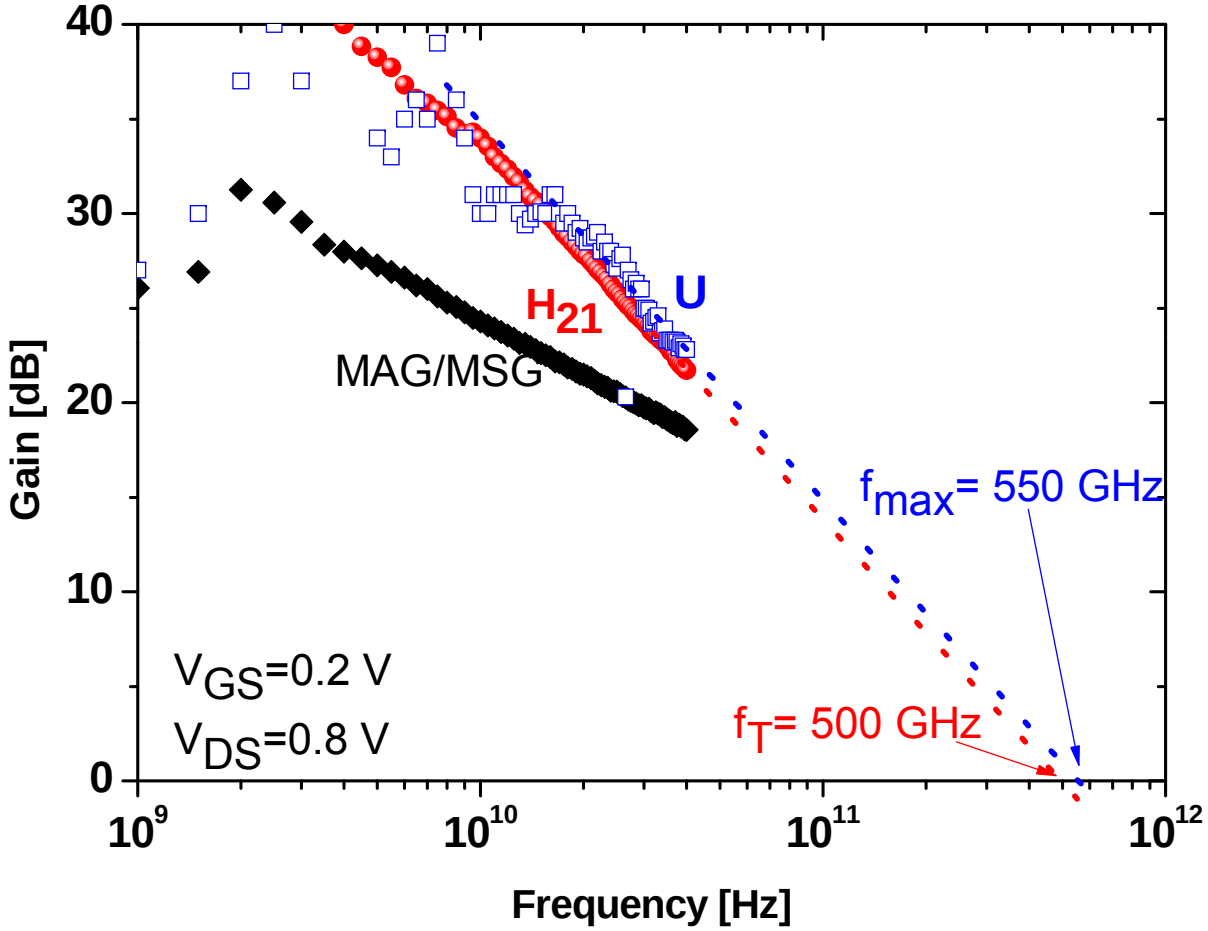
Subthreshold Char. : L_g = 30 nm



- DIBL = 118 mV/V, S = 83 mV/dec.
- Excellent I_{OFF}

➔ I_{ON}/I_{OFF}= 3.9 X 10^4 for V_{DS} = 0.5 V

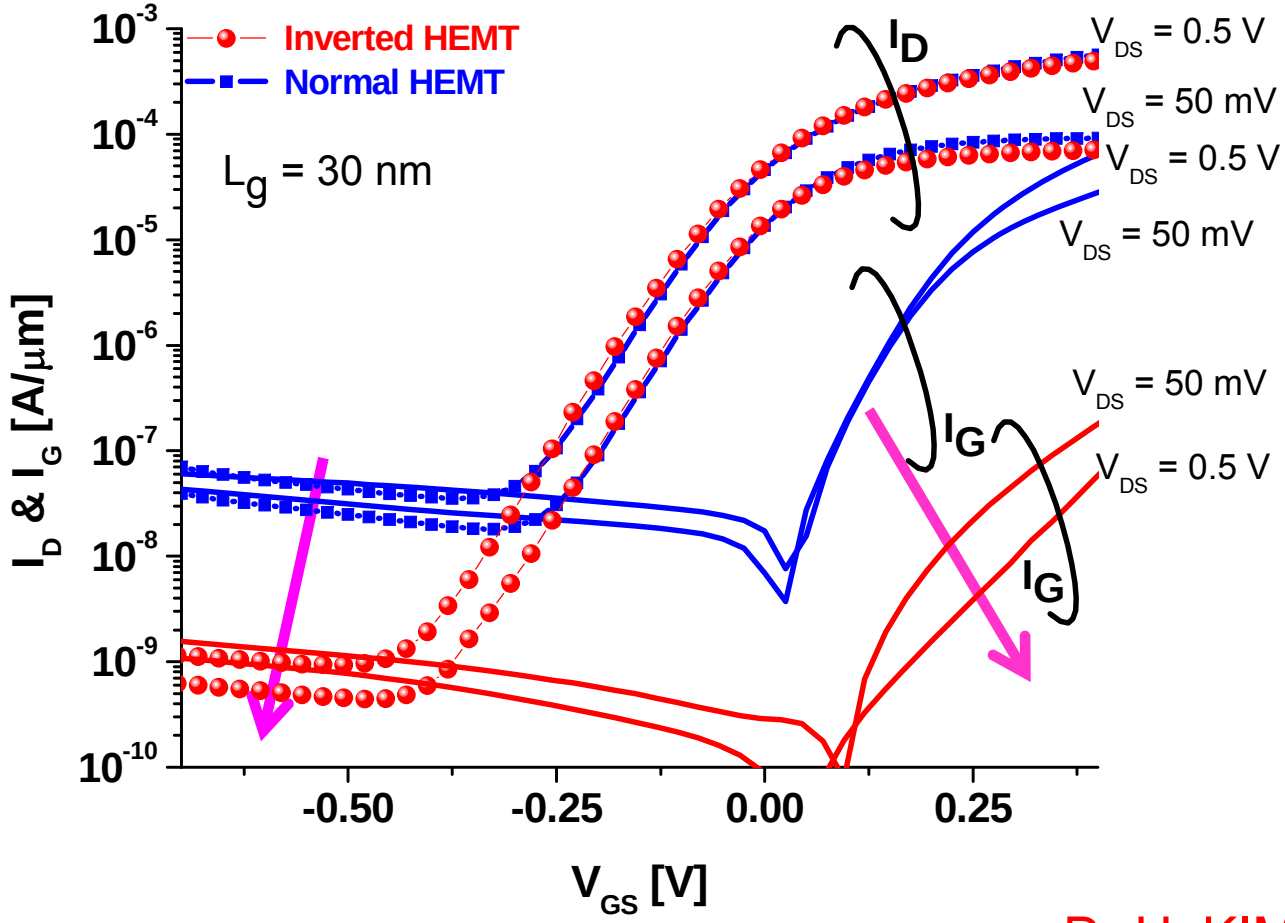
f_T & f_{max} Char. : L_g = 30 nm



f_T=500 GHz & f_{max}=550 GHz

Highest f_T & f_{max} reported on Inverted HEMTs

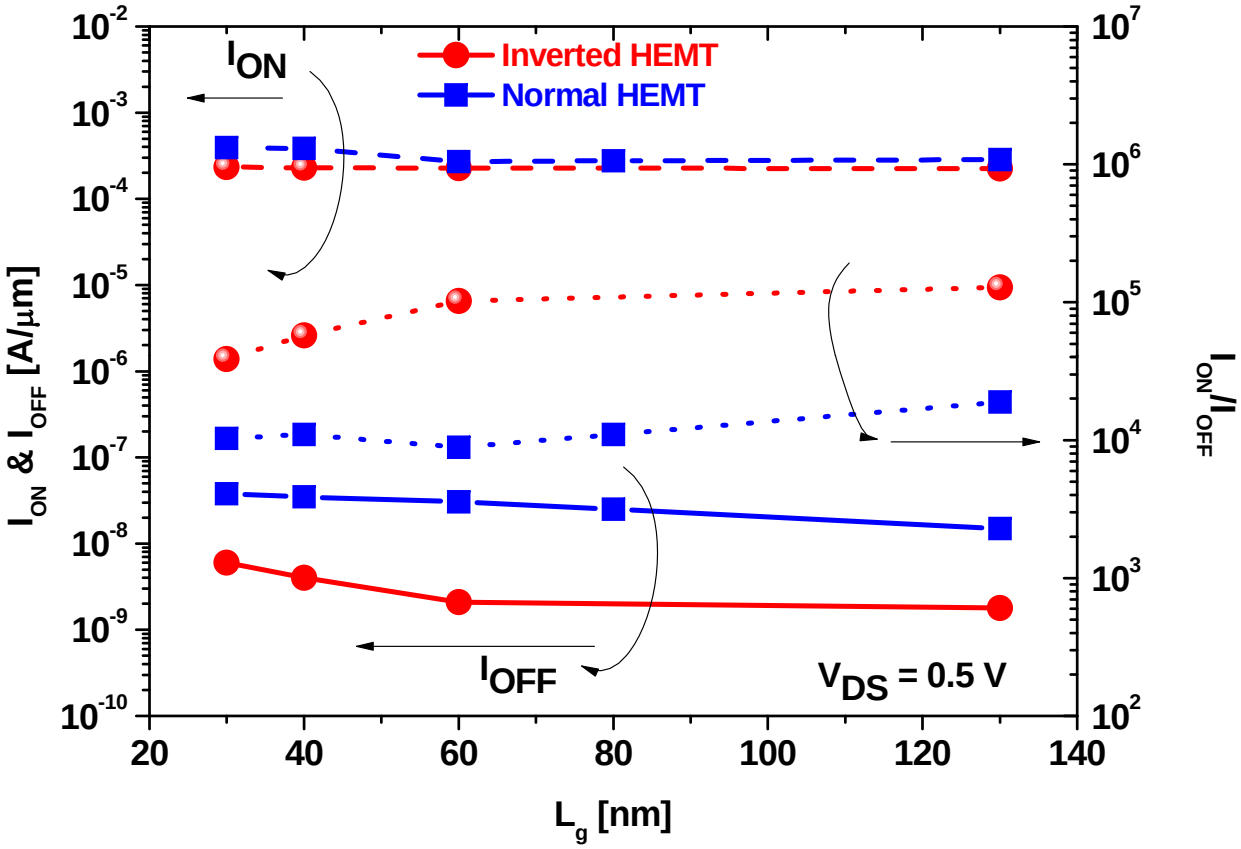
Inverted vs. Normal HEMTs: I_G



<D.-H. KIM IPRM 09>

Inverted HEMT: ➔ ~100 X less I_G than normal HEMT

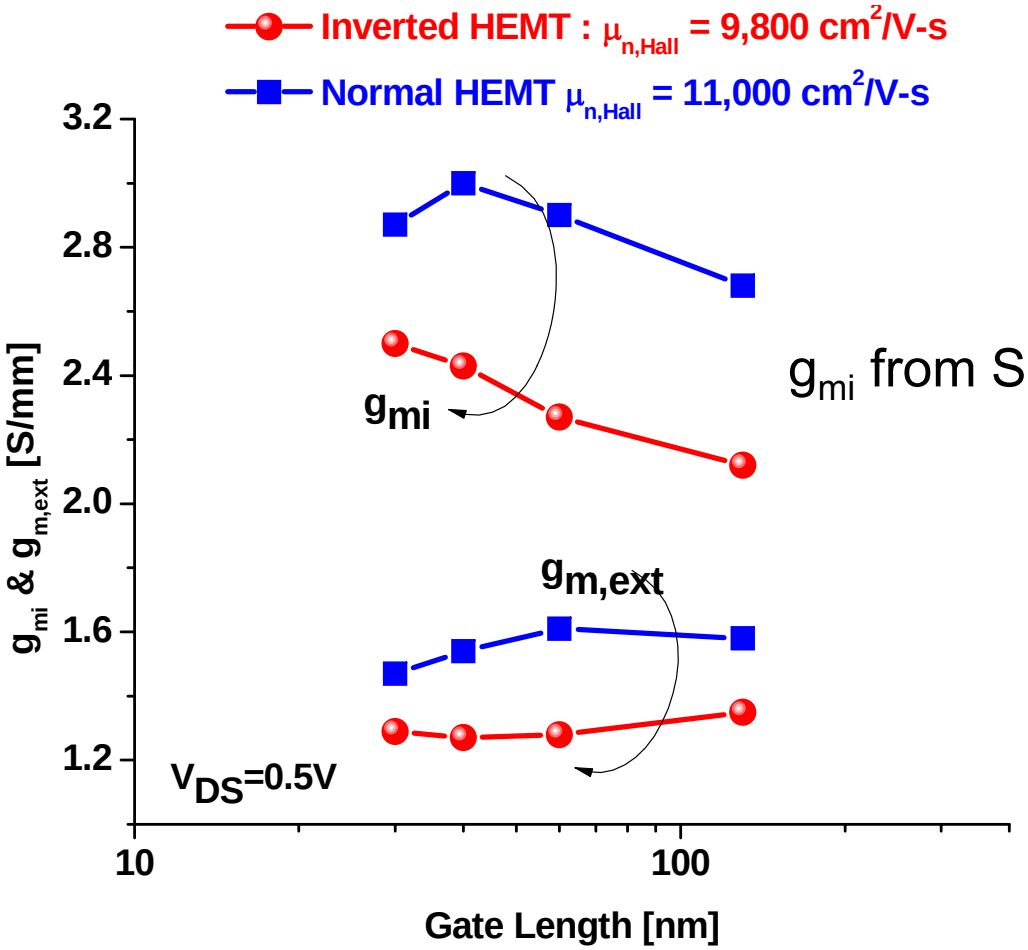
Inverted vs. Normal HEMTs: I_{ON}/I_{OFF} vs. L_g



Inverted HEMT:

⇒ Excellent I_{ON}/I_{OFF} scalability down to L_g = 30 nm

Inverted vs. Normal HEMTs: g_{mi}



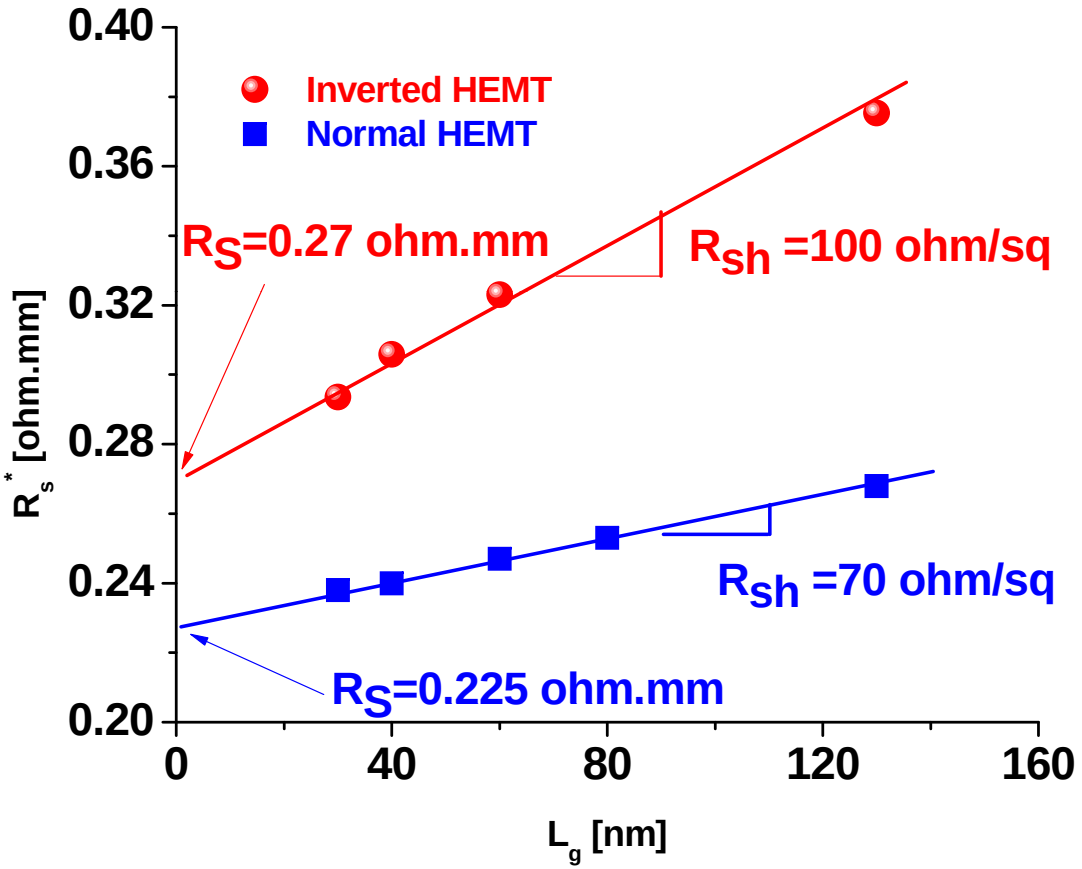
g_{mi} from S-parameters

Inverted HEMTs:

- Lower values of g_{mi}: from reduced μ and velocity
- Better g_{mi} scalability down to 30 nm

Inverted vs. Normal HEMTs: R_s

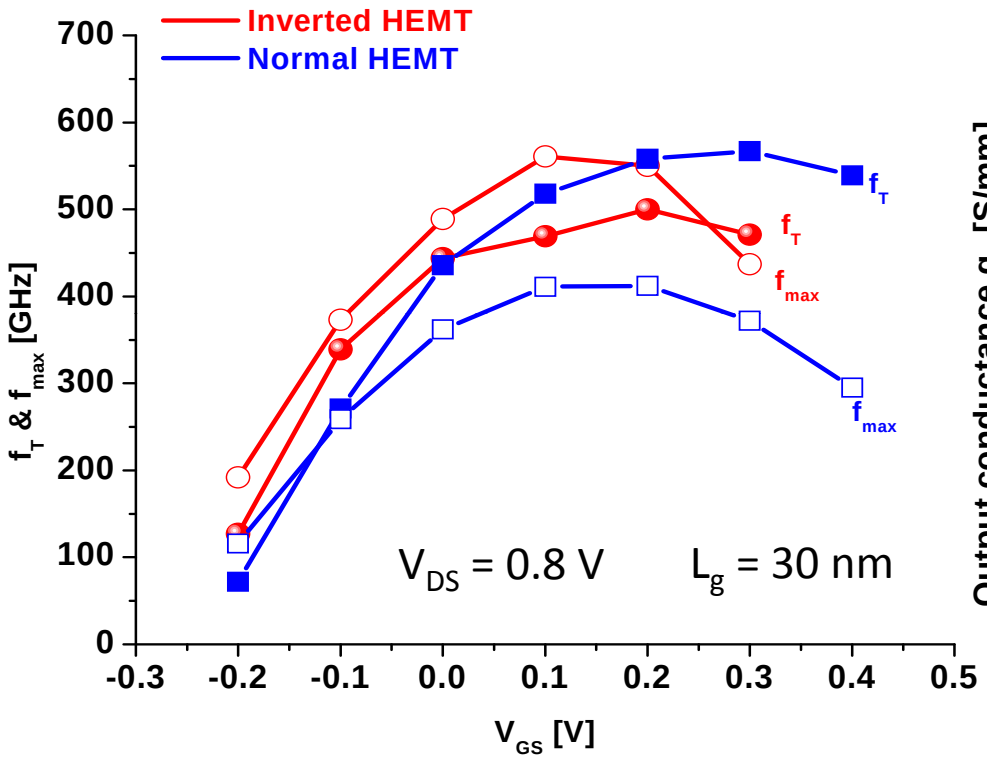
<Using gate current injection technique>

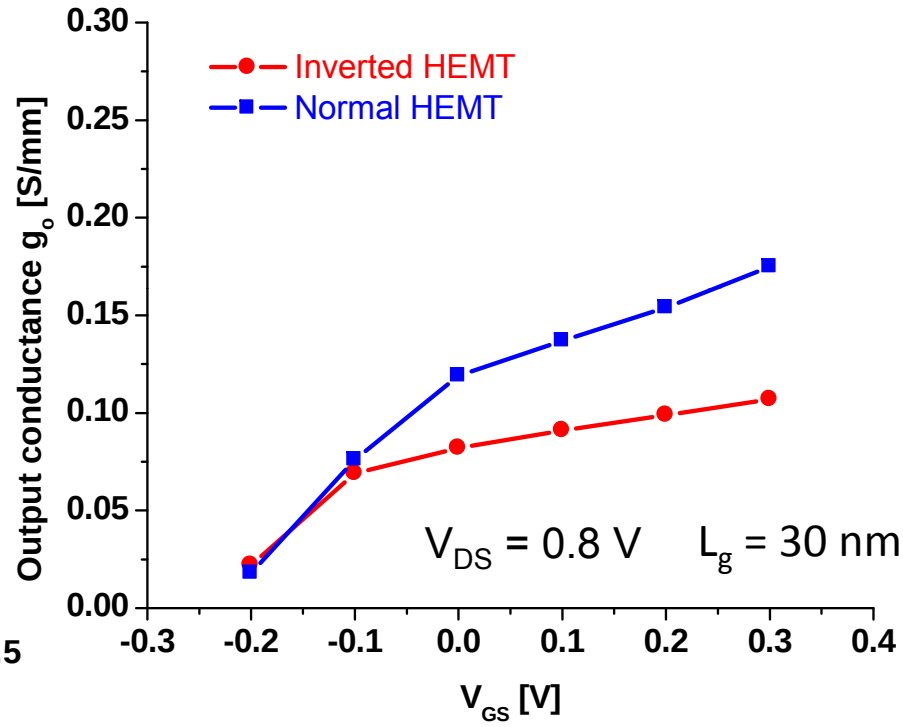


Higher R_s in inverted HEMT

Why? ➔ Lower n_s in access region, higher R_c

Inverted vs. Normal HEMTs: f_T and f_{max}

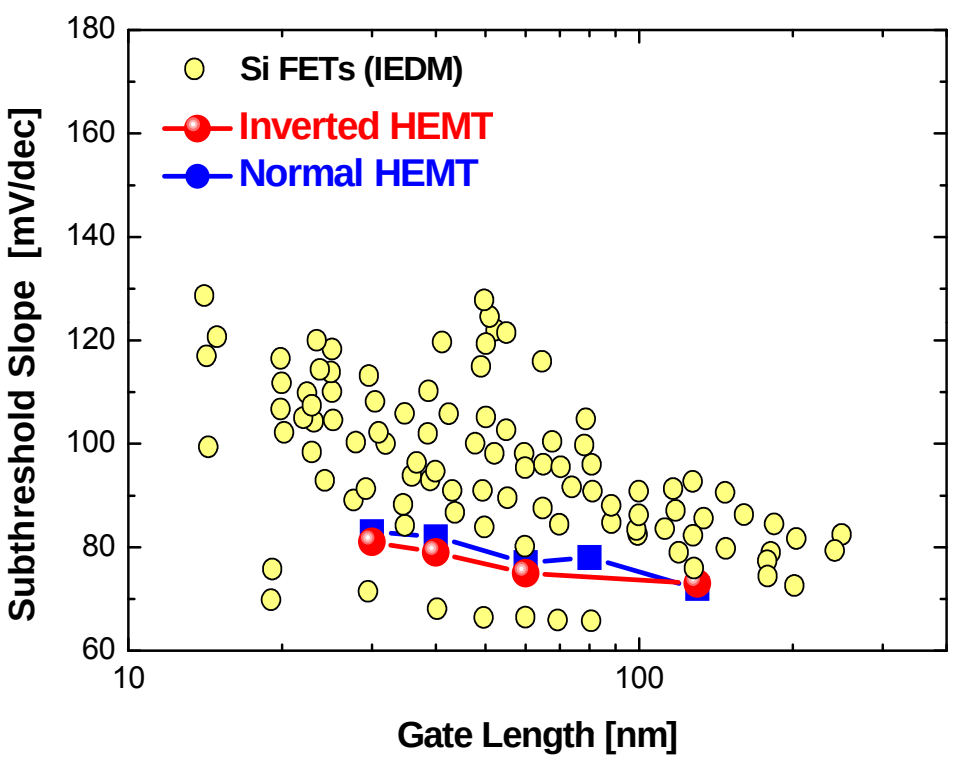


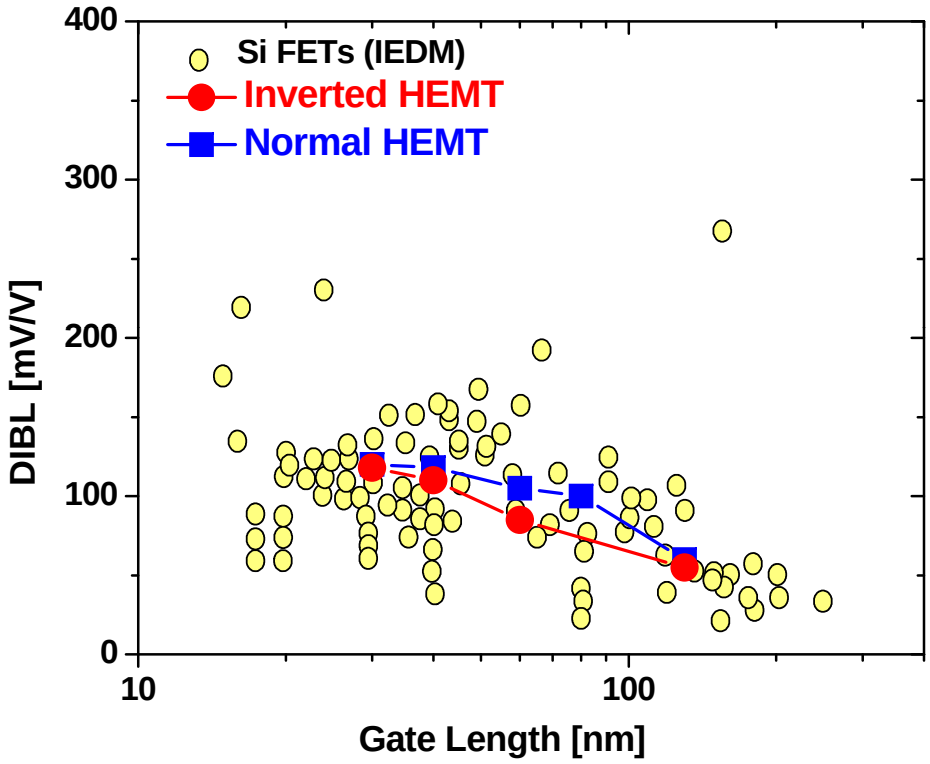


Inverted HEMTs:

- ➔ Lower f_T & higher f_{max}
- ➔ Improved g_o: possibly due to lower n_s in access region

Benchmarking : SS & DIBL

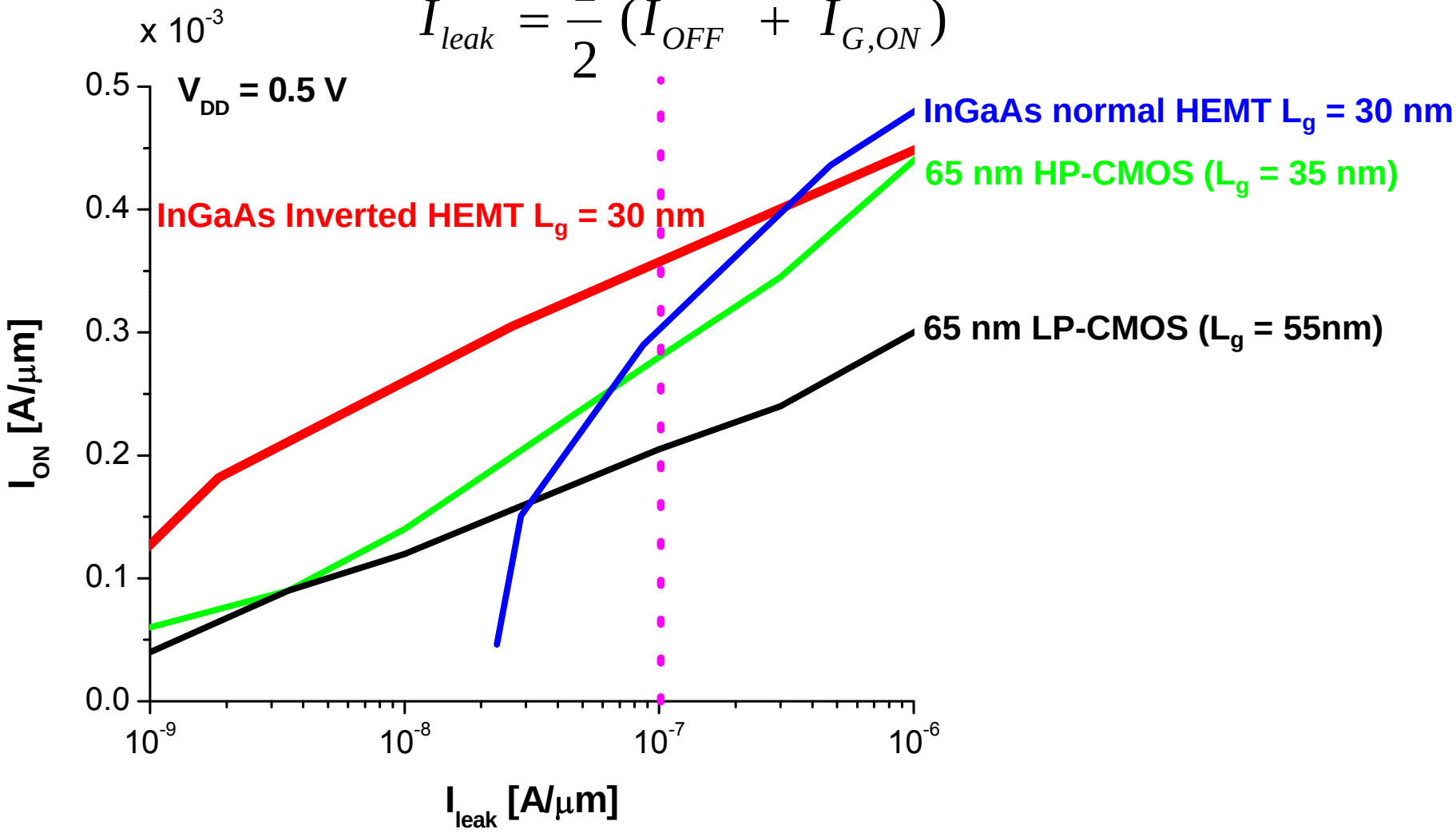




Excellent SCE of inverted HEMT

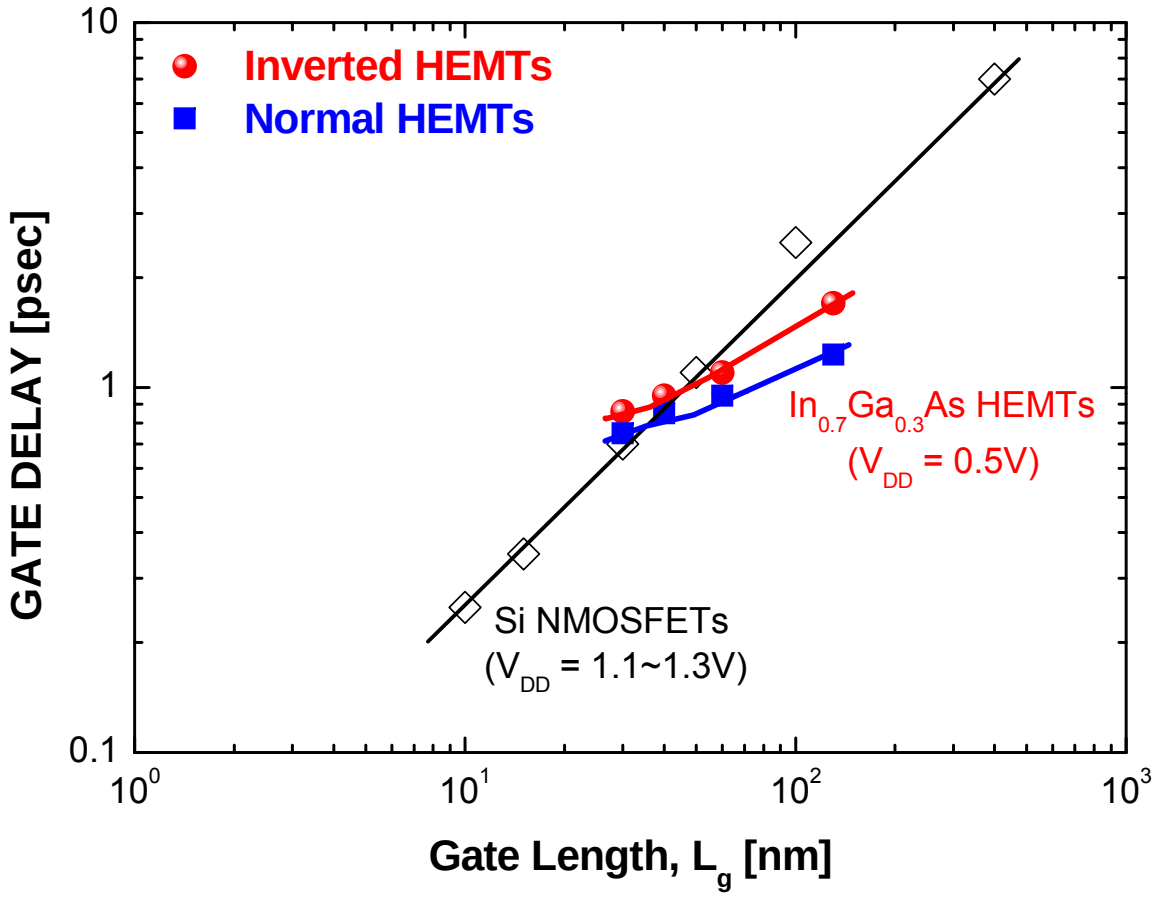
Benchmarking : I_{ON} vs. I_{Leak}

$$I_{leak} = \frac{1}{2}(I_{OFF} + I_{G,ON})$$



➔ At I_{leak} = 100 nA/μm, **1.3X** higher I_{ON} than 65 nm HP CMOS

Benchmarking : CV / I vs. L_g



Inverted HEMT:

$\Rightarrow$ Comparable Gate delay with L_g but at lower V_{DD}

< Ref. : Chau *et al.* (T-Nano 2005) >

Conclusions

- **Inverted InGaAs HEMT**
  - Scaling benefit:
    - Reduced I_g → allows for further L_g scaling
  - At 30 nm, inverted HEMTs exhibit excellent characteristics:
    - DIBL < 120 mV/V, S < 85 mV/dec and I_{ON}/I_{OFF} ~ 4 x 10^4
    - f_T > 500 GHz and f_{max} > 550 GHz, CV/I ~ 1 psec

- **Inverted InGaAs HEMT: promising layer structure for future high-K/III-V MOSFET**